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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,872	11/08/2001	John Lin	BP 1907	5330

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EXAMINER
DOAN, DUC T

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,872	LIN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/9/2006 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). ✓

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set for in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 11/29/2005 has been entered.

Claims 1-22 have been presented for examination in this application. In response to the last Office Action, none of the claims were amended. None of the claims were added. As a result, claims 1-22 are now pending in this application.

Claims 1-22 are rejected.

Applicant's arguments filed 12/27/2005 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the remarks.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 16-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013) and in view of Loyer (US 4652874).

As for claim 1, Auckland describes a wireless transceiver device, comprising: modulation circuitry for modulating and demodulating signals that are transmitted over the airwaves (Fig 1: #100); frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals (Fig 1: #100); digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog (Fig 1: #100) [The RF/IF section 104 includes a receive module 110, a transmit module 112 and a frequency synthesizer 114. The receive module 110 generally includes a low noise amplifier (LNA), frequency downconversion, filtering, demodulation, analog to analog to digital conversion, etc., as indicated in FIG. 1.The transmit module 112 generally includes a frequency upconversion, filter, digital to analog conversion and modulation as indicated in FIG. 1;Auckland's paragraph 4, lines 1-8]; a radio controller (Fig 1: #100) [The radio 100 includes a digital or baseband section 102, a radio frequency-to-intermediate frequency (RF/IF) section 104 and a radio frequency (RF) section 106;Auckland's paragraph 2, lines 1-2]; and baseband processing circuitry (Fig 1: #108 DSP) . Auckland describes the base-band section including a processor (Fig 1: DSP) to process data being received and being tranmitted. Auckand further describes an embodiment with multiple data ports being processed (Auckand's paragraph 55). Auckand does not describe the memory structure for storing addresses for accessing data blocks. However, Loyer describes a frame descriptor queue that functioning as a first in, first out memory structure (Fig 6: queue FD lists) capable of storing the addresses associated with data to be transferred

(Fig 6: data buffer) [a pointer to the associated BD, and a pointer to the next element on FD queue; Loyer's column 9, lines 33-34]. It would have been obvious to one of ordinary skill in the art at the time of invention to include memory structures as suggested by Loyer in Auckland's system to dynamically allocate buffers to appropriate queues for faster processing data being received and being transmitted. (Loyer's column 10, lines 6-7).

As for claims 2-4 and 8-10 correspondingly, the rejection in claim 1 is incorporated herein. The claims recite the wireless transceiver of claim 1 further including a plurality of command blocks (Fig 6: queue FD lists) formed within a memory structure, which command blocks include addresses of data blocks stored within random access memory [a pointer to the associated BD, and a pointer to the next element on FD queue; Loyer's column 9, lines 33-34]; wherein the first in, first out memory structure includes pointers that define addresses of the command blocks (The FD contains a frame descriptor, and a pointer to the next element in the FD queue); further forming a memory portion for storing an indicator for indicating whether a command block is in use [Also, TBC 10 maintains status indicators and command response information within this table; Loyer's column 9, lines 9-10; the ram based structured that TBC using corresponds to the claim's forming a memory portion].

As for claim 5, Auckland describes the wireless transceiver of claim 1 wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry [The radio may support any type of carrier modulation such as frequency modulation (FM), gaussian phase shift keying (GPSK), gaussian mean shift keying (GMSK), quadraduture amplitude modulation (QAM) or other scheme now know or later developed; Auckland's paragraph 147, lines 2-4].

As for claim 6, the claim recites the wireless transceiver of claim 1 wherein the frequency conversion circuitry converts directly between radio frequency and baseband. Auckland describes an ACU capable of tuning to operate at different frequencies (Auckland's paragraph 76, lines 10-12); Frequency information come from baseband processor (Fig 6, DSP #614) [The ACU 606 receives frequency, timing, and possibly other control signals at an input 628 from the synthesizer 612, or from the controller 614 as indicated by the dashed line in the drawing figure].

As for claims 7, the claim recites storing a data block in random access memory; and storing a pointer that corresponds to the data block in a first in, first out memory structure (Loyer's Fig 6, page 9 lines 30-40 FD queue has pointer to the element on the FD queue).

As for claims 11 and 12, the claims recite the method of claim 10 wherein an address for a data block is only stored in a command block if an indicator reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted; including the step of evaluating a command block address stored within a FIFO pointer; including the step of resetting the indicator signal if the transmission was successful. Loyer teaches frame descriptors (with associated data blocks) being removed when frames are sent out [For transmission the host processor adds frame descriptors (messages) to a transmit queue and TBC 10 removes them as they are sent out; Loyer's column 9, lines 32-33].

As for claim 16, it is rejected based on the same reason as in claim 11.

Claim 17 rejected based on the same rationale as in the rejection of claim 7.

As for claim 18, it is rejected based on the same rational as in claim 2.

As for claim 19, it is rejected based on the same rational as in claim 4.

As for claim 22, Auckland describes the memory structure of claim 17 wherein the first in, first out memory structure defines a plurality of first in, first out memory blocks (Fig 6: Frame descriptor blocks) wherein each first in, first out memory relates to data blocks (Fig 6: Frame Buffers) that are to be transmitted to a particular device (destination address; Auckland's column 9, lines 30-33).

Claims 13-15,20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013) as applied to claims 13,17 respectively, and in view of Loyer (US 4652874) and further in view of Firoozmand (US 5136582).

As for claims 13-15, the claims recite the method of claim 12 further including examining the contents of the command block specified by the pointer to determine a data block address; including the step of evaluating at least the first memory location of the data block (Firoozmand's Fig 13: Frm 1 length) whose address is specified in the command block to determine the size of the data block; including the step of retrieving an amount of data corresponding to the size data block specified in claim 14 and transmitting that data to a radio modem for transmission over a wireless airwaves. Auckland and Loyer do not describe the claim's detail description on size of the data block. However, Firoozmand describes the length field located at first memory location (Firoozmand's Fig 13: Frm 1 length, bits 0 to 15). It would have been obvious to one of ordinary skill in the art at the time of invention to include length field as suggested by Firoozmand in Auckland's system to quickly calculate the length of data block when packet is being received [Establishing locations of receive buffers is more complex. Whereas the length of transmit packets is common and known and their locations in memory

also are known, receive packets can be variable in length and locations must be defined dynamically as receive packets arrive from the network; Firoozmand's column 15, lines 34-38].

As for claims 20 and 21, Firoozmand describes the memory portions for storing the indicators are each one bit in length (Firoozmand's Fig 20: long word 1 LW1) [Buffer status bits include an OWN bit that is set by the host processor to signify that this entry is a valid entry for the DMA controller 124 to use, and that the DMA controller "owns" the descriptor; Firoozmand's column 13, lines 60-62]; wherein the memory portions for storing the command blocks are each four bytes in length (Firoozmand's Fig 20: long word 2 LW2).

Response to Arguments

Applicant's arguments filed in response to the previous Office Action have been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

As to the remarks on page 5-7, Aukland teaches features of the wireless transceiver device as described in claim 1, such as frequency conversion circuitry, digital-to-analog conversion circuitry, a radio controller, and a baseband processing circuit. Aukland does not describe the memory structure's detail of the claim. Auckand further describes an embodiment with multiple data ports being processed (Auckand's paragraph 55). Auckand does not describe the memory structure for storing addresses for accessing data blocks.However Loyer clearly describes a memory structure comprises of a frame descriptor queue that functioning as the claims's first in first out memory data structure for storing addresses for accessing data block (Loyer's Fig 6, queue FD list points to FD which is a link list of data buffer which corresponding to the claims's data block; Loyer's column 9, lines 30-40). Loyer clearly describes the functions

of the frame descriptors and buffer descriptors in a RAM based structure (Loyer's column 9, lines 5-22) to store addresses for accessing data block (Loyer's column 9, lines 15-19, lines 60-64). Loyer describes, "the buffer management structure is powerful and flexible. The frame descriptors can be generated independently of the message content and link the frame descriptor to the buffer descriptor list without altering the buffer descriptor. This scheme also makes very efficiently use of memory space"; Thus it's advantageously to use the request and data queues as taught by Loyer into Auckland's system to store requests from different sources (transmiting, receiving, multiple data ports) such that the base-band processor (Auckland's Fig 1: DSP) can provides execution in an efficiently manner (dynamically allocate buffers to appropriate queues for faster processing data being received and being transmitted; Loyer's column 10, lines 6-7). Examiner notes an equivalent description of such a memory structure is found in the specification page 22, lines 3-12.

As for the remark on page 9, for claim 7, Examiner respectfully disagrees. As discussed in above paragraphs, the frame descriptors are stored in a queue. Because of the queue structure, they will be executed in the FIFO first in first out order.

As to the remark on page 6 that there is no motivation to apply the memory structure taught by Loyer, Examiner respectfully disagrees. As discuss in the above paragraph, Loyer describe the flexibility and independent of the frame descriptors and the message content. Loyer clearly describes the quick and efficiently way of linking the frame descriptor to allocated buffers without altering the allocated buffers (Loyer's column 10, lines 3-10). Because of the above flexibility, the frame descriptors can be further grouped into appropriated queue (Loyer's column 10, lines 6-7).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watanabe (US 6148336) describes a detail of a command descriptor block (Fig 3,4). Queues data structures in memory including pointers to data block and tag for command data blocks.

Ono (US Pub 2001/0049769) describes processing units with cache controllers and queues processing in parallel manner.

Bose (US 6654428) describes multiple FIFO for transmitting and receiving data to be processed by DSP hardware. Multiple buffer rings are maintained in memory.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan 1/19/06

Supervisory Patent Examiner

TC2188

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SUPERVISORY PATENT EXAMINER